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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,928	10/28/2003	Isao Okada	Q78036	4142

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EXAMINER	
BIBBINS, LATANYA	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,928	OKADA ET AL.	
	Examiner	Art Unit	
	LaTanya Bibbins	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/15/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following minor informality: the word "form" should be changed to "from." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 10, 11, 13, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5, 10, 11, 13, and 14 recite the limitation "the multiplexer." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Iijima (US PGPub 2002/0051415 A1).

Claim 1 recites a recording pulse generator comprising a delay line having plural circuit elements cascaded in multiple stages, a means that generates plural fine clocks that each have a different phase than the clock inputted to the first stage of the delay line, a means that selects an arbitrary fine clock from the plural fine clocks generated, and a recording pulse generation means that generates a recording pulse on the basis of a fine clock selected.

The means plus function language recited in claim 1 indicates that applicant intends to invoke 35 U.S.C. 112 paragraph six. Where means plus function language is used, claim limitations are interpreted to read on only the corresponding structure disclosed in the specification and equivalents thereof. The disclosed structures used for the "means that generates plural fine clocks," "means that selects an arbitrary fine clock," and the "recording pulse generation means" are a delay line, a multiplexer, and a flip-flop circuit respectively.

Iijima discloses a recording waveform generator that includes a delay line with a plurality of delay elements connected in series which receives a first clock signal, a selector for selecting one delay clock signal from the delay clock signal group and a recording waveform generation circuit that receives a data signal and processes the data signal in synchronization with the delay clock signal in order to generate a recording waveform signal **(see paragraph [0014] and Figures 1 and 3)**. Iijima further discloses that the delay clock signal group is a set of signals each having a different phase difference from the first clock signal **(see paragraph [0033])**.

The delay line, selector, and recording waveform generation circuit taught in Iijima are structural equivalents of the delay line, multiplexer, and a flip-flop circuit

disclosed in the specification. That is, the delay line, selector, and recording waveform generation circuit taught in the prior art are capable of performing the functions specified in the claim in the same manner as the delay line, multiplexer, and flip-flop disclosed in the specification. Therefore, the prior art elements are deemed equivalent and the claimed limitations are met by the prior art.

Claim 4 is drawn to the recording pulse generator of claim 1 where the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks. Iijima discloses a selector for selecting one delay clock signal from the delay clock signal group **(see paragraph [0014] and Figures 1 and 3)**. A selector is a switch that connects multiple lines to a single line and as such is equivalent to a multiplexer. Both components are used in the execution of conditional logic such as memory addressing and device selection and signaling.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima as applied to claims 1 and 4 above, and further in view of Hayashi et al. (US Patent Number 6,493,305 B1). See the teachings of Iijima above.

Claims 2, 3, and 6-9 are drawn to the recording pulse generator further comprising a phase locked loop (PLL) oscillator and an eight to fourteen (EFM) clock that is inputted to the first stage of the first delay line. The PLL oscillator has an oscillator with plural circuit elements cascaded in multiple stages, compares the phase of the signal generated by the oscillator with the phase of the clock inputted to the first stage, and controls a voltage of a power supply line according to the phase comparison result where the first delay line is connected to the common power supply line of the oscillator and the circuit elements are equivalent to the circuit elements of the oscillator.

Iijima discloses a PLL oscillator and a clock inputted to the first stage of the first delay line but does not teach the specifics of the PLL oscillator or an EFM clock that varies according to a recording speed. However, Hayashi et al. teaches a pulse width control circuit with a PLL oscillator having a voltage controlled oscillator (VCO), phase comparator, and a low pass filter that supplies a control voltage. The VCO of the PLL circuit includes a plurality of delay cells connected in series **(see column 9 lines 58 and 59 and Figure 9).** The phase comparator compares the phase of the oscillator output and the reference signal **(see column 9 lines 48-52).** The low pass filter of the PLL oscillator supplies a control voltage, Vt, according to the phase difference signal **(see column 9 lines 52-54).** The control voltage, Vt, from the low pass filter is supplied to the control terminal of both delay cells and both delay cells have the same circuit elements and configuration **(see column 9 lines 66 and 67, column 10 lines 1-5 and Figure 9).** Hayashi et al. also teaches an EFM clock that varies according to recording speed **(column 1 lines 40-42).**

It is apparent that one of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima with Hayashi and would have had a reasonable expectation in producing the claimed invention because Iijima and Hayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a PLL oscillator and a delay circuit with common circuit elements and a common supply voltage as described by Hayashi. Hayashi provides motivation for using a common supply voltage (column 1 lines 49 and 50 and in column 10 lines 7-10) by stating that the delay circuit is sensitive to external effects such as power fluctuations and that the delay cells of the VCO and the delay cells of the delay line are arranged to be in close proximity. It would have also been obvious to one of ordinary skill in the art, at the time the invention was made, to use an EFM clock input because EFM reduces errors by minimizing the number of zero-to-one and one-to-zero transitions and small pits and lands are avoided. Disks can be played or written at different speeds; therefore the EFM data needs to be written to the disk at different speeds. As the speed increases, the period of the EFM signal decreases. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Claims 5 and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima and Hayashi as applied to claims1-4 and 6-9 above, and further in view of Kobayashi et al. (US Patent Number 5,818,805). See the teachings of Iijima and Hayashi above.

Claims 5 and 10-16 are drawn to a recording pulse generator where the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

Iijima and Hayashi disclose a recording waveform generation circuit that processes data based on a delayed clock signal that is supplied from a selector but do not specifically teach the elements of the circuit. However, Kobayashi teaches a recording signal generating apparatus that uses a T-type flip-flop that is triggered by the output of a data selector **(see Figure 16 element 18 and column 12 lines 50 and 51)**. The data selector provides one of eight delayed clock outputs to the T-type flip-flop **(see Figure 16 element 10 and column 12 lines 28-36)**.

It is apparent that one of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima and Hayashi with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, Hayashi, and Kobayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Bibbins whose telephone number is (571) 270-1125. The examiner can normally be reached on Monday through Friday 7:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shanon Foley can be reached on 571 272-0898. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Bibbins
Patent Examiner

Shanon Foley
Supervisory Patent Examiner